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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,968	03/31/2004	Kyo-Min Sohn	8021-225JHM/SS18860US	8696

22150 7590 01/22/2008

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	
MAIL DATE	**DELIVERY MODE**
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,968	SOHN ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/2/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12,15 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21* is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/814,968, the Examiner acknowledges the applicant's submission of the amendment dated November 2, 2007. At this point, claims 1 and 12 have been amended and claims 4, 13-14, 16-20 and 22 stand canceled. There are 13 claims pending in the application; there are 3 independent claims and 10 dependent claims, all of which are ready for examination by the examiner. Claims 1-3, 5-12, 15 and 21 are pending.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1-3, and 5-11** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "the data memory address" in line 10. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read **–a data memory address-**.

5. Any claims not specifically addressed above are rejected for encompassing deficiencies found in base claims upon which they depend.

REJECTIONS BASED ON PRIOR ART

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claims 1 and 12** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14 and 19 respectively of copending Applications No. 10/811,613, now patented as US 7,193,903.

2. Initially, it should be noted that the present application and Application No. 10/811,613, now patented as US 7,193,903 have the same inventive entity. The assignee for both applications is Samsung Electronics Co., Ltd.

3. Claimed subject matter in the instant application is fully disclosed in the referenced US patent and would be covered by any patent granted on that copending application since the referenced US patent and the instant application are claiming common subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

4. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of US patents 7,193,903 in the instant application. See MPEP § 804.

5. Claim 1 is compared to claim 14 of application 10/811,613 in the following table:

Instant Application	**Application 10/811,613**
1. (Currently Amended) An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:	1. (Currently Amended) A method of controlling an integrated circuit (IC) to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal
a plurality of memory blocks, each of the memory blocks Comprising a plurality of sub-memory blocks;	and which comprises a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks,
a plurality of data memory blocks corresponding to the memory blocks, wherein each of the data memory blocks has the same size as a sub-memory block;	data memory blocks corresponding to the memory blocks,

and a tag memory controlling unit,	and a tag memory controlling unit, the method comprising:
which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein when the write address and the read address are the same as the data memory address, the read operation, is performed in the data memory block and the write operation is performed in the sub-memory block, and wherein when the write address and the read address are both not the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the operation corresponding to the address that is not the same as tile data memory address is performed in the sub-memory block.	(a) receiving a write address, a read address, and write data; (b) determining, a memory block and a data memory block in which a data read operation and a data write operation are to be performed in response to the write address and the read address; (c) performing the data read operation or the data write operation in the data memory block according to the determination of step (b); and (d) performing the data read operation or the data write operation in the memory block according to the determination of step (b). 14. (Currently Amended) The method of claim 1, wherein the tag memory controlling unit writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address.

6. Claim 12 is compared to claim 19 of application 10/811,613 in the following table:

Instant Application	Application 10/811,613
12. A method for simultaneously performing a write operation and a read operation in an integrated circuit having a separate input and output and a plurality of data memory blocks and a plurality of sub-memory blocks, the method comprising:	15. (Currently Amended) A method for performing a write operation and a read operation in an integrated circuit (IC) comprising a separate input and output (I/O), a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks, data memory blocks corresponding to the memory blocks, and a memory controlling unit, the method comprising: receiving a write address, a read address and a write data command during a period of a clock signal;
determining if a write address and a read address have been input during a period of a clock signal;	determining, a first memory location and a second memory location, where a write operation and a read operation are to be performed in response to the write address and the read address; and performing the write operation in one of the first memory location and the second memory location and the read

	operation in one of the first memory location and the second memory location. 18. (Original) The method of claim 15, wherein the determination step further comprises: determining if the write address and the read address are input;
determining if an upper address of the write address is the same as an upper address of the read address, when the write address and the read address have been input during the period of the clock signal;	determining if an upper address of the write address is coincident with an upper address of the read address; determining if the write address and the read address are coincident with a data memory address; and determining if data stored in one of the first memory location and the second memory location is valid data.
and performing a write operation and a read operation such that upon determining that the write address and the read address are the same as a data memory address, the read operation is performed in the data memory block and the	19. (Original) The method of claim 18, wherein the performing step further comprises: performing the write operation or the read operation in one of the first memory location and the second memory location, when the

write operation is performed in the sub-memory block and upon , determining that the write address and the read address are both not the same as the data memory address the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block.	operation to be performed corresponds to the address coincident with the data memory address; performing the read operation in one of the first memory location and second memory location, when the write address and the read address are coincident with the data memory address; storing new data in one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is valid data; and writing the new data to one of the first memory location and the second memory location, when data stored in one of the first memory location and the second memory location is not valid data.

This double patenting rejection applies to dependent claims 2-3, 5-11 and 15.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

6. Applicant's arguments filed on November 2, 2007 have been considered and are partially persuasive.

7. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

8. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

FIRST POINT OF ARGUMENT

9. Applicant's remarks with respect to 35 U.S.C. 101 and 112 rejections are persuasive as the prior 35 U.S.C. 101 and 112 rejections have been overcome by claim amendments presented on amendments and arguments filed on November 2, 2007; therefore, previously presented 35 U.S.C. 101 and 112 rejections have been withdrawn.

SECOND POINT OF ARGUMENT

10. In response to Applicant's remarks with respect to obviousness-type double patenting rejection under US Application 10/811,613, now patented as US 7,193,903 wherein Applicant remarks that the instant application and US Application 10/811,613, now patented as US 7,193,903 "cannot cover the same subject matter, since a method claim does not infringe an apparatus claim;" the Examiner disagrees.

11. There Examiner would like to respectfully submit that type double patenting rejection of the instant application under US Application 10/811,613, now patented as US 7,193,903 is deemed proper since M.P.E.P. 821.04 [R-3] reads "Where applicant voluntarily presents claims to the product and process, for example, in separate applications (i.e., no restriction requirement was made by the Office), and one of the applications issues as a patent, the remaining application

may be rejected under the doctrine of obviousness-type double patenting, where appropriate (see MPEP 804 -804.03), and applicant may overcome the rejection by the filing of a terminal disclaimer under 37 CFR 1.312 (c) where appropriate" **[See M.P.E.P. 804.01 [R-3] and M.P.E.P. 821.04 [R-3]]**.

THIRD POINT OF ARGUMENT

12. Applicant's remarks with respect to the double patenting rejection under US 6,826,088 are persuasive as the prior double patenting rejection under US 6,826,088 has been overcome by claim amendments and arguments filed on November 2, 2007; therefore, previously presented double patenting rejection under US 6,826,088 has been withdrawn.

FOURTH POINT OF ARGUMENT

13. Applicant's remarks with respect to Liu in view of Favor in light of claim amendments presented on November 2, 2007 is found to be persuasive; therefore, the rejection of claims 1-3, 8-13 and 15 under 35 U.S.C. 103 has been withdrawn.

14. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated November 2, 2007.

CLOSING COMMENTS

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

17. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

18. The subject matter of claims 1-3, 5-12, 15 and 21 is considered as allowable subject matter; however, claims 1-3, 5-12, and 15 stand rejected as obviousness-type double patenting under application 10/811,613, now issued as patent US 7,193,903 (See above).

19. The primary reasons for allowance of claims 1 and 12 in the instant application is the combination with the inclusion in these claims of the limitation of method/system for simultaneously performing a write operation and a read operation wherein "**when the write address and the read address are the same as the data memory address, the read operation, is performed in the data memory block and the write operation is performed in the sub-memory block., and wherein when the write address and the read address are both not the same as the data memory address, the operation corresponding to the address that is the same as the data memory address is performed in the data memory block and the**

operation corresponding to the address that is not the same as the data memory address is performed in the sub-memory block." The prior art of record neither anticipates nor renders obvious the above recited combination.

20. The primary reasons for allowance of claim 21 in the instant application is the combination with the inclusion in these claims of the limitation of an integrated circuit for simultaneously performing a write operation and a read operation wherein "**a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same, wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks and a number of columns and rows different from a number of columns and rows of the data memory blocks**." The prior art of record neither anticipates nor renders obvious the above recited combination.

a(2) CLAIMS REJECTED IN THE APPLICATION

21. Per the instant office action, claims 1-3, 6, 8-13, and 15 have received a second action on the merits and are subject of a final rejection.

a(3) CLAIMS NO LONGER UNDER CONSIDERATION

22. Claims 4, 13-14, 16-20 and 22 stand canceled as of amendment received on November 2, 2007.

b. DIRECTION OF FUTURE CORRESPONDENCES

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

24. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 8, 2008

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100